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A THOROUGH INVESTIGATION OF DYNAMIC BIAS ON LINEAR GaAs FET POWER AMPLIFIER PERFORMANCE

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ABSTRACT

Methods which involve increasing the gate bias on GaAs power FETs at reduced input power levels are excellent techniques for increasing efficiency. This paper presents the results of a thorough study on the effects of dynamic gate bias on GaAs power FET performance. Detailed information concerning the effects of gate bias changes on gain, input return loss, and linearity are included. A two-stage linear power amplifier was built and tested that successfully demonstrated dynamic gate bias optimization. This amplifier produced over 5 Watts of output power at L-Band with high efficiency and excellent linearity.

INTRODUCTION

GaAs FET power amplifiers operating at or near 1 dB compression exhibit high efficiencies but have poor linearity. For this reason, low distortion linear power amplifiers must operate below or backed off from compression. These amplifiers exhibit rather poor efficiency at reduced drive levels since the DC power consumption remains constant while the output power decreases.

Methods for improving the efficiency of GaAs FET linear power amplifiers with varying input signal levels have been described in the literature.(1), (2) The method providing the greatest efficiency improvement over a large input power range uses dynamic gate biasing to decrease the DC power consumption at reduced drive levels. This technique has been described and compared in a theoretical sense to other classes of operation (i.e., class A, A\B and B), but the effects of dynamic biasing on other amplifier performance parameters such as input return loss, gain, and linearity have not been examined.

This paper examines the effects of dynamic gate biasing on the principle performance parameters - output power, power-added efficiency, linearity, gain, and input return loss - of a linear power GaAs FET amplifier and presents the results of a rigorous parametric investigation. The results of the investigation were then used to demonstrate a L-band high performance 5 Watt two-stage linear power amplifier. For testing and demonstration purposes, dynamic gate bias adjustment was obtained by manual control of the gate voltage at pre-determined intervals over the input RF drive level. A practical implementation would employ an automatic method for gate voltage adjustment as a function of drive level.

DEVICE CHARACTERIZATION

Intermodulation distortion (IMD) levels between -30 and -40 dBc can typically be achieved at 3 to 4 dB back-off from 1 dB compression. Therefore, to obtain 5 Watt linear operation a 10 Watt FET was selected.

A test set combining load-pull and IMD measurement capabilities was developed for FET characterization. The test set was used to find the optimal device source and load impedances for maximum output power and minimum return loss, as well as to assess the effects of reduced input power and bias changes on output power, gain, efficiency, return loss and linearity. A diagram
set is shown in Figure 1.

With the FET mounted on a
in the test set and biased for
1 dB compression, the output power and input

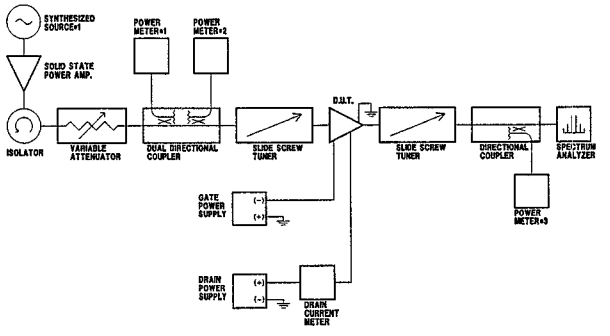

Figure 1: A customized load-pull test system was used to characterize the devices.

return loss were optimized by adjusting the input and output tuners. Using these optimum matching conditions, the device output power, gain, power-added efficiency, return loss, and linearity were measured at different gate bias voltages over an input power range of 11 to 30 dBm. The results of the measurements, shown in Figures 2, 3 and 4, reveal several important device characteristics.

First, as the gate bias becomes more negative, the device output power, gain and dissipated power decrease at any given input power level. This occurs because the device transconductance also decreases proportionally with drain current.

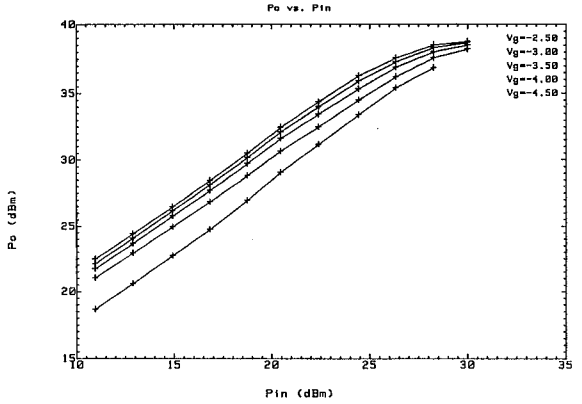

Figure 2: The output power decreases with more negative gate bias on the FET.

Second, the device input return loss remains within acceptable limits except at gate bias voltages near pinch-off. This is very important because the device input match is not adversely affected by gate bias and input power level changes. This aspect has not been addressed previously for linear amplifiers employing dynamic gate biasing.

Third, the power-added efficiency increases at low drive levels as the gate is

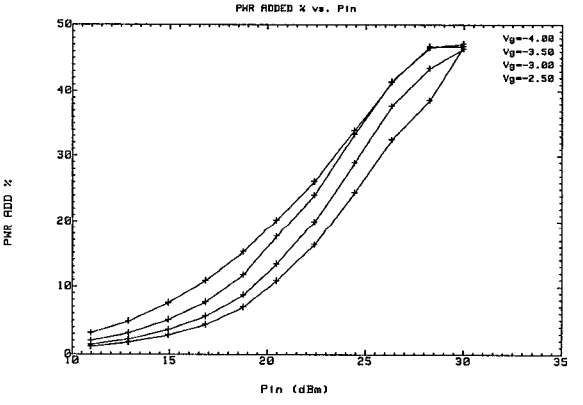

Figure 3: The power-added efficiency increases with more negative gate bias until pinch-off is approached.

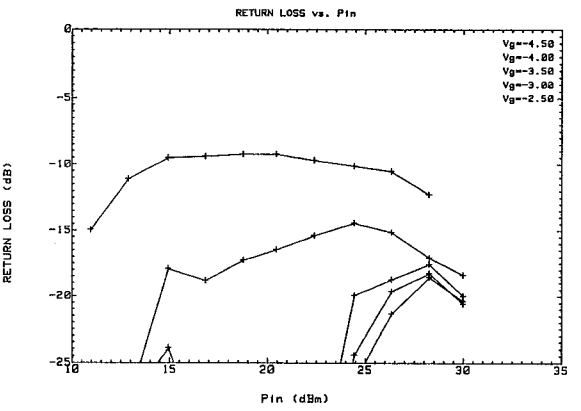

Figure 4: The return loss of the "matched" FET degrades with increased negative gate bias until pinch-off.

biased more negatively. These changes in the device performance as a function of gate bias make it possible to obtain significantly improved efficiencies in linear power amplifiers at low drive levels.

FIVE WATT LINEAR OUTPUT STAGE

The design of the output stage made use of the parametric data collected during the device characterization process. The output stage matching network impedances were optimized at 3 dB back-off for best performance over the input power level range. The output stage bias and matching networks were fabricated and assembled on ceramic-loaded dielectric/aluminum laminate. A photograph of the completed output stage is shown in Figure 5.

Measurements were conducte
stage as a function of gate b
level to maximize performan
specific dynamic bias cases. Cc

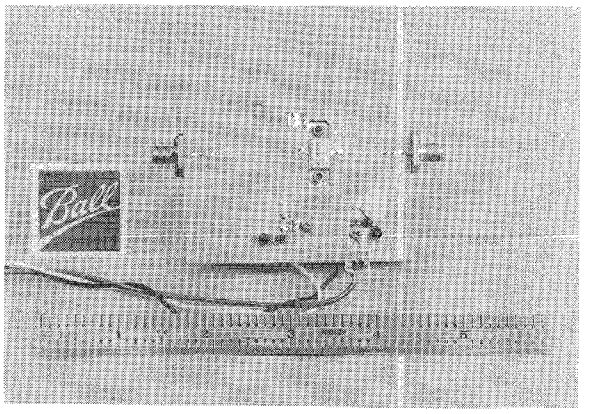

Figure 5: The five Watt output stage was optimized for high efficiency and low distortion.

gain was a requirement for each of the three cases. The *full power* bias case used a single gate voltage setting to achieve the highest output power over the input power range. The *optimum efficiency* case used carefully selected gate bias voltages at specific input power levels to produce the highest possible power-added efficiency. For the *optimum IMD* dynamic bias case, gate bias voltages were chosen for maximum third-order IMD levels of -30 dBc and the highest possible efficiency. The power-added efficiencies for the three bias cases are plotted in Figure 6.

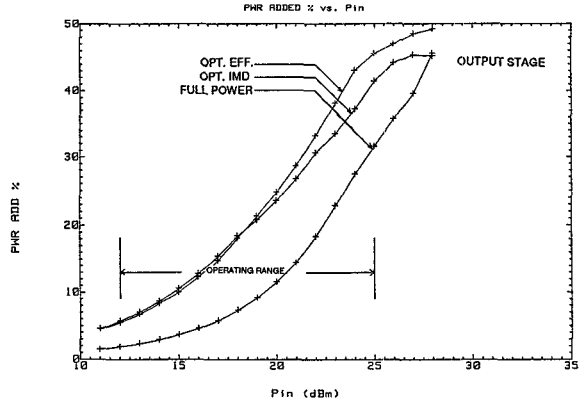

Figure 6: Dynamic biasing improves the power-added efficiency associated with the *full power* bias case.

The *optimum efficiency* dynamic biasing approach increases the average efficiency by about ten percent over *full power* bias. Comparisons between the three bias cases for power consumption, input return loss and third-order IMD (IMD_3) performance are presented in Figures 7, 8 and 9, respectively. The use of dynamic biasing greatly reduces the power consumption while maintaining typically better than 15 dB input return loss and -30 dBc IMD_3.

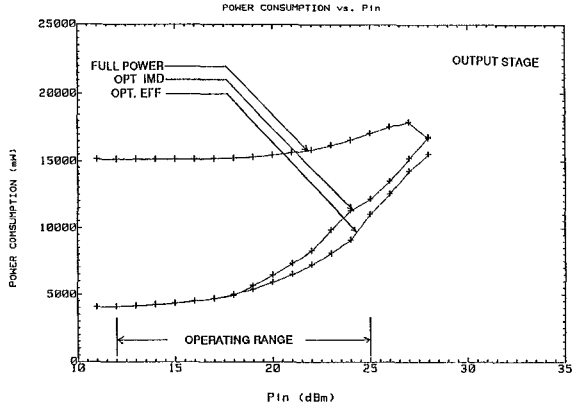

Figure 7: Both dynamic biasing approaches greatly reduce DC power consumption.

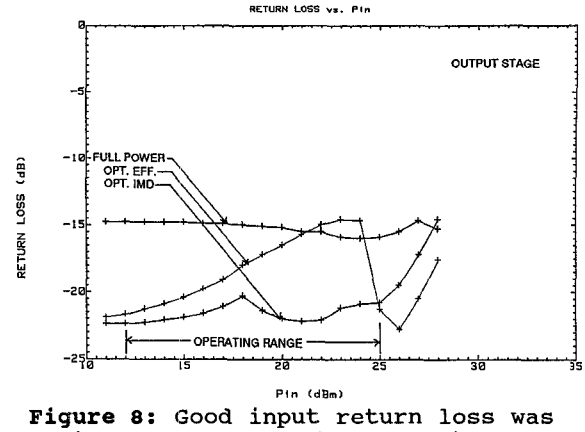

Figure 8: Good input return loss was achieved for each of the three bias cases over the input power range.

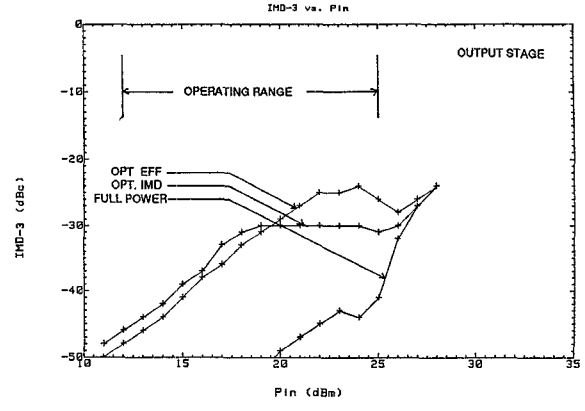

Figure 9: The trade-off between optimum efficiency and IMD_3 is evident when comparing the linearity of the three bias cases.

TWO-STAGE AMPLIFII

A high performance two-stage linear amplifier employing the above output device and a driver stage both using dynamic gate bias was developed and tested. For measurements conducted on this amplifier, the *optimum IMD* dynamic biasing method was utilized for both stages. The *optimum IMD* bias tuning provided the highest efficiency while still maintaining the desired -30 dBc IMD_3 level. The desired 5 Watt output power level was achieved at 4 dB back-off from 1 dB compression. Moreover, at 3 dB back-off a 6.1 Watt level was obtained while achieving the -30 dBc maximum IMD_3 level. A plot of the output power versus input power is given in Figure 10. The two-stage power amplifier maintained a constant gain of 30 dB over the input power operating range. Using *optimum IMD* biasing, the amplifier exhibited better than -30 dBc

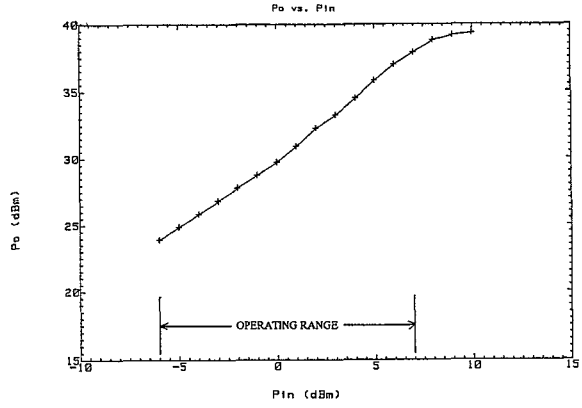

Figure 10: The two-stage amplifier was optimized for output power, efficiency and linearity.

IMD_3 over the 13 dB input power range as shown in Figure 11. The two-stage amplifier provided this linearity with a power-added efficiency of better than 33% at the maximum operating drive level as is shown in Figure 12. A minimum power-added efficiency of about 4% was obtained at the lowest input drive

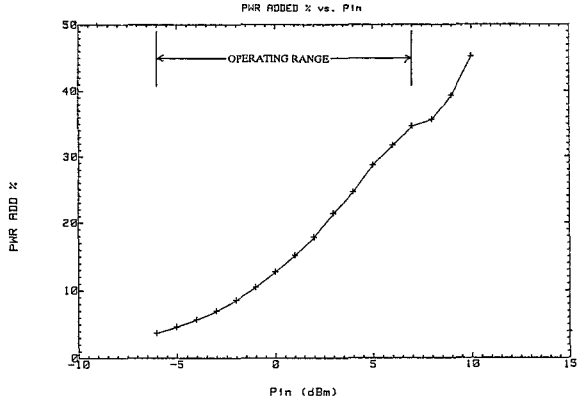

Figure 11: The two-stage amplifier was simultaneously tuned for linearity and efficiency.

level. Even though 4 percent power-added efficiency may seem low, it represents a dramatic improvement over the *full power* bias approach. By using *optimum IMD* biasing, the DC power consumption is reduced by over 70 percent. Therefore, rather than drawing over 20 Watts of DC power at low drive levels, the two-stage amplifier draws only 6.5 Watts. The linearity of the power amplifier can be improved to levels below -30 dBc IMD_3 at the expense of decreased efficiency or increased power consumption. In addition, the linearity can be improved by operating the amplifier at a greater input back-off level; however, this too sacrifices efficiency. Dynamic biasing provides an extra degree of freedom to operate a linear amplifier at a higher efficiency and lower intermodulation distortion level than would otherwise be possible using only input power back-off.

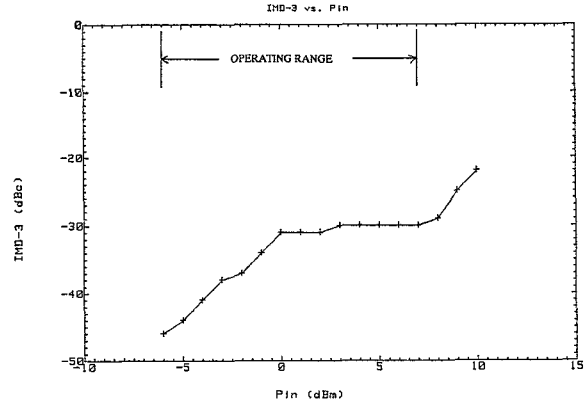

Figure 12: The two-stage amplifier bias was optimized for an IMD_3 of less than -30 dBc.

CONCLUSION

The investigation into the effects of gate bias and input power changes on the performance of a L-band GaAs power FET shows that significant reductions in the power consumption of a linear power amplifier can be obtained over a wide input power range using a dynamic gate biasing technique without adversely affecting input return loss and gain. Using a manual gate bias control for dynamic gate bias adjustment, a power GaAs FET exhibited 6 Watts output, -30 dBc IMD_3, better than 20 dB input return loss, and a maximum power-added efficiency of 43 percent. A two-stage demonstration amplifier provided similar results with a gain
maximum power-added efficiency

ACKNOWLEDGEMENT

This work was partially funded by the Satellite Communications Div. of Motorola, Inc.

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(2) A.M. Saleh and D.C. Cox, "Improving the Power-Added Efficiency of FET Amplifiers Operating with Varying-Envelope Signals, "IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-31, No. 1, pp. 51-56, January 1983.